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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,733	03/03/2004	Shih-Lun Chen	3111-426	2650

7590 05/12/2005

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EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 05/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EF

Office Action Summary	Application No.	Applicant(s)	
	10/790,733	CHEN ET AL.	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-12* is/are rejected.

7)☒ Claim(s) *9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The limitation recites "a 1V NMOS transistor" is vague and indefinite. There is no definition given for 1V NMOS transistor. Clarification is required.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, 5-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Clark (6,201,428).

Clark shows:

1. An output buffer with low-voltage devices to driver high-voltage signals (Fig. 6 & 6), comprising:

a tri-state control circuit (622, 624, 626), capable of receiving and processing external low-voltage signals and high-voltage signals and outputting at least two resulting signals;

a level converter (N61-62, P66-67, P610-611), connected to the tri-state control circuit by one end thereof, for receiving the resulting signals so as to convert low-voltage swing to high-voltage swing;

an output end module (104, Fig. 2), consisting of a plurality of serial-connected metal-oxide semiconductor field effect transistors (P21-22, N21-22);

a first taper buffer (N63-64, P68-69, P612-P13), having one end connecting to the level converter and another end thereof connecting to the output end module; and

a second taper buffer (5 inverters of 620 outputting an Pdown signal 210), having one end connecting to the tri-state control circuit and another end thereof connecting to the output end module.

2. The output buffer with low-voltage devices of claim 1, wherein the maximum voltage receivable by the plural MOSFETS (P21, N22, & N21) is 2.5V.

3. The output buffer with low-voltage devices of claim 1, wherein the buffer is capable of driving high-voltage signals for PCI-X output applications (PCI bus col. 8, line 31).

5. The output buffer with low-voltage devices of claim 1, wherein the output buffer is designed in a 0.13 ft m 1V/2.5V CMOS process.

6. The output buffer with low-voltage devices of claim 1, wherein the tri-state output buffer consists of a CMOS NAND gate (622 & 626) and a CMOS NOR gate (624).

7. The output buffer with low-voltage devices of claim 1, wherein the PMOS and NMOS transistors of the first taper buffer are 2.5V nominal Vt transistor (N63-64, P68-69, P612-P13 are normal MOSFETs with have threshold about .7 - .8 volt).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4-5, 8, 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clark (6,201,428).

4. Clark discloses the claimed invention except for the output buffer is operating between 133 MHz and 66 MHz in PCI environment. It would have been obvious to one having ordinary skill in the art at the time the invention was made to operate the output buffer between 133 MHz and 66 MHz, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art.

5. Clark discloses the claimed invention except for the output buffer is designed in a 0.13um 1V/2.5V CMOS process. It would have been an obvious matter of design choice to design the output buffer in a 0.13um 1V/2.5V CMOS process, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art.

8. Clark discloses the PMOS and NMOS transistors of the second taper buffer are 1.8 V nominal Vt transistors, therefore Clark disclose the claimed invention except for the PMOS and NMOS transistors of the second taper buffer are 1V nominal Vt transistors. It would have been obvious to one having ordinary skill in the art at the time

the invention was made to provide the PMOS and NMOS transistors of the second taper buffer are 1V nominal Vt transistors, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art.

11-12. Clark discloses the claimed invention except for the swing voltage of the first taper buffer is 1V – 3.3V and the second taper buffer is 0V – 1V. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the swing voltage of the first taper buffer is 1V – 3.3V and the second taper buffer is 0V – 1V, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art.

Allowable Subject Matter

5. Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH Q. TRAN
PRIMARY EXAMINER

5/6/05